



OKAYA Electric America, Inc.

### SPECIFICATIONS

SAMPLE CODE \_\_\_\_\_

MASS PRODUCTION CODE \_\_\_\_\_

RH240320L-2X4NN-O

DRAWING NO. \_\_\_\_\_

**Customer Approved**

**Date:**

Sales Sign	QC Confirmed	Checked By	Designer

Approval For Specifications Only.

\* This specification is subject to change without notice.

Approval For Specifications and Sample.



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## Contents

### 1. SPECIFICATIONS

- 1.1 Features
- 1.2 Mechanical Specifications
- 1.3 Absolute Maximum ratings
- 1.4 DC Electrical Characteristics
- 1.5 Electro-Optical Characteristic

### 2. MODULE STRUCTURE

- 2.1 Counter Drawing
- 2.2 Interface Pin Description
- 2.3 Timing Characteristics

### 3. QUALITY ASSURANCE SYSTEM

- 3.1 Quality Assurance Flow Chart

### 4. RELIABILITY TEST

- 4.1 Reliability Test Condition

### 5. PRECAUTION RELATING PRODUCT HANDLING

- 5.1 Safety
- 5.2 Handling
- 5.3 Storage
- 5.4 Terms of Warranty

### 6. PACKING Specification

See Appendix 2

Appendix :

- 1. LCM drawing
- 2. LCM Packaging Specifications

Note : For detailed information please refer to IC data sheet : Samsung --- S6E63D6

## 1. SPECIFICATIONS

### 1.1 Features

Item	Standard Value
Display Type	240 * (RGB) * 320 Dots
LCD Type	OLED
Color Mode	Full Color (262K color)
Driver Mode	Active Matrix
Screen size(inch)	2.4(Diagonal)
Interface	MPU i80-system 18-/16-9-8-Bit bus interface MPU i68-system 18-/16-9-8-Bit bus interface Serial data transfer interface RGB 18-/16-/6-bit bus interface(DOTCLK, VSYNC, HSYNC, DE, DB17-0)
Controller IC	Driver IC : Samsung --- S6E63D6
ROHS	THIS PRODUCT CONFORMS TO ROHS

### 1.2 Mechanical Specifications

Item	Standard Value	Unit
Outline Dimension	42.6 (W) * 59.2 (L) * 1.65 (H)	mm

#### OLED panel

Item	Standard Value	Unit
Active Area	36.72 (W) * 48.96 (L)	mm

Note : For detailed information please refer to LCM drawing

### 1.3 Absolute Maximum ratings:

Items	Symbol	Unit	Value	Note
Power supply voltage 1	VDD3	V	-0.3~+5.0	
Power supply voltage 2	VCI	V	-0.3~+5.0	
Supply Voltage range	VLIN2-VLIN3	V	20	
Input Voltage range	Vin	V	-0.3~VDD+0.5	

Note:

- (1) Absolute maximum rating is the limit value. When the IC is exposed operation environment beyond this range, the IC do not assure operations and may be damaged permanently, not be able to be recovered.
- (2) Absolute maximum rating is guaranteed only when our company's package used.

## 1.4 DC Electrical Characteristics

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Driving voltage	VGH	-	3.0	-	8.0	V	
	VGL		-8.0	-	-3.0	V	
	VINT		-4.0	-	-1.0	V	
Logic Operating Voltage	RVDD	-	1.45	1.5	1.55	V	
Operating frequency	Fose	Frame frequency=60Hz Display line=320 line	1161.1	1290.2	1419.3	KHz	
1 <sup>st</sup> step-up input voltage	VCI1	-	2.1	-	2.75	V	
1 <sup>st</sup> step-up output voltage	VLOUT1	Without load	+4.6	-	+5.5	V	
1 <sup>st</sup> step-up output efficiency	VLOUT1	I_VLOUT1_LOAD=2.3mA	90	95	-	%	
2 <sup>nd</sup> step-up output voltage	VLOUT2	Without load		8.1		V	
2 <sup>nd</sup> step-up output efficiency	VLOUT2	I_VLOUT2_LOAD=0.1mA	90	93	-	%	
3 <sup>rd</sup> step-up output voltage	VLOUT3	Without load	-	-10.6	-	V	
3 <sup>rd</sup> step-up output efficiency	VLOUT3	I_VLOUT3_LOAD=0.1mA	90	93	-	%	
Source Output voltage deviation (channel to channel)	-	-	-	+/-TBD	-	mV	
Output voltage deviation (Chip to Chip)	-	-	-	+/-TBD	-	mV	
Source driver output Voltage range	Vso	-	0.96	-	4.2	V	

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
LTPS driver output voltage deviation	-	-	-	-	TBD	V	
Driving voltage	dVGH	Voltage deviation	-	-	TBD	V	
	dVGL		-	-	TBD	V	
Current consumption during normal operation	IVDD3	No load, Ta=25°C VCI=2.8V Frame(f)=60Hz	-	-	TBD	uA	-
	IVCI		-	-	TBD	mA	-

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Power supply Voltage	VCI	Operating Voltage	2.5	2.8	3.3	V	
Power Supply Voltage	VDD3	I/O supply voltage	1.65	1.8	3.3	V	
Logic High level input voltage	V <sub>IH</sub>		0.7*VDD3		VDD3	V	
Logic Low level input voltage	V <sub>IL</sub>		0		0.3*VDD3	V	
Logic High level output voltage	V <sub>OH</sub>	I <sub>CUT</sub> =-1mA	0.8*VDD3		VDD3	V	
Logic Low level output voltage	V <sub>OL</sub>	I <sub>CUT</sub> =+1mA	0		0.2*VDD3	V	

## 1.5 Electro- Optical Characteristics

Items	Symbol	Min.	Typ.	Max	Unit	Remark
Operating Luminance	L		200	-	Cd/ m <sup>2</sup>	(1)(5)
Power Consumption	Pon	-	260	-	mW	30% Pixels on(1)
Response Time	Tres	-	-	50	US	(2)
CIE <sub>x</sub> (White)	W <sub>x</sub>	0.26	0.30	0.34	-	(5)
CIE <sub>y</sub> (White)	W <sub>y</sub>	0.30	0.34	0.38	-	(5)
Viewing Angle	VA	170	-			(3)
Contrast	CR	-	10000:1			(4)
Operation Lifetime	L <sub>top</sub>	10000			Hrs	(1)(6)
Storage lifetime	L <sub>Ts</sub>	20000	-	-	Hrs	(7)

Note:

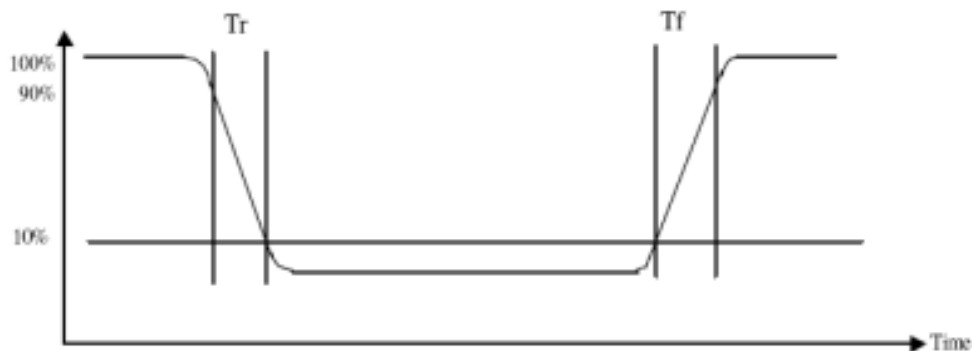
Measuring surrounding :dark room

Surrounding Temperature:25°C

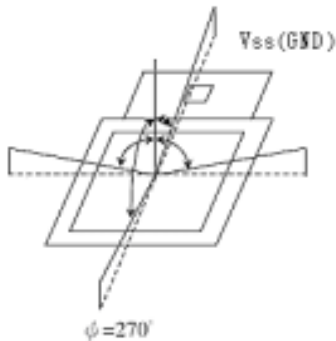
1. Test condition:

TBD

2.response Time test condition



3. Viewing Angle test condition:



4. Contrast

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

5. Optical tester: Topcon SR3

6. Full white with check board at 85Hz frame rate, 1/96 duty. Operating Life Time is defined when the luminance has decayed to less than 50% of the initial measured luminance before life test.

7. The storage life time is define as 50% when the luminance has decayed to less than 50% of the minimum luminance under temperature  $25^\circ\text{C}$ ,  $\text{RH} < 50\%$ .

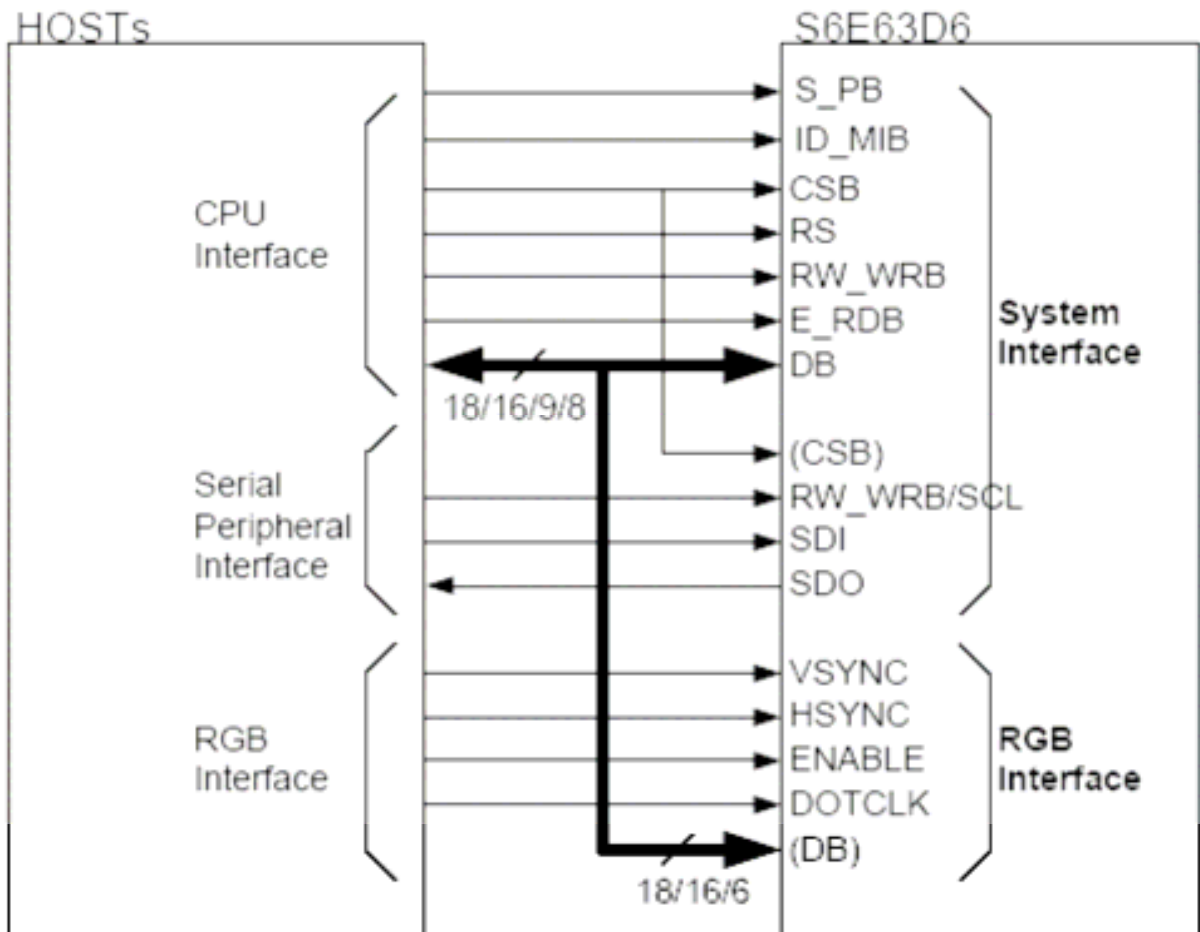
## 2. MODULE STRUCTURE

### 2.1 Counter Drawing

#### 2.1.1 LCM Mechanical Diagram

\* See Appendix

#### 2.1.2 Block Diagram



## 2.2 Interface Pin Description

Pin No.	Symbol	Function
1	AR_VDD	Positive voltage for OLED.
2	AR_VSS	Negative voltage for OLED.
3	VCI	Power supply for analog circuit(2.5v~3.3v).
4	VCI1	A reference voltage for 1 <sup>st</sup> booster.
5	GND	Ground.
6	C12M	External capacitance connect pin between C12M and C12P.
7	C12P	
8	C11M	External capacitance connect pin between C11M and C11P.
9	C11P	
10	VLOUT1	1 <sup>st</sup> booster output pin.
11	C31P	External capacitance connect pin between C31M and C31P.
12	C31M	
13	C32P	External capacitance connect pin between C32M and C32P.
14	C32M	
15	VLOUT3	3 <sup>st</sup> booster output pin.
16	VLOUT2	2 <sup>nd</sup> booster output pin.
17	C21P	External capacitance connect pin between C21M and C21P.
18	C21M	
19	VGS	A reference level for the grayscale voltage generation circuit.
20	IOVCC	I/O power supply.
21	SPB	Select the CPU interface mode.(0=parallel interface,1=serial interface).
22	ID_MIB	Select the CPU type.(0=intel 80x-system,1= intel 68x-system).
23	DB17	Operates liked an 18-bit bi-directional data bus. 18-bits bus I/F: DB17-0
24	DB16	
25	DB15	
26	DB14	

Pin No.	Symbol	Function																				
27	DB13	BI-directional data bus. When CPU I/F, 18-bit interface:DB 17-0 16-bit interface:DB 17-10,DB 8-1 9-bit interface:DB 8-0 8-bit interface:DB 8-1 When RGB I/F 18-bit interface:DB 17-0 18-bit interface:DB 17-0 16-bit interface:DB 17-10,DB 8-1 6-bit interface:DB 8-3																				
28	DB12																					
29	DB11																					
30	DB10																					
31	DB9																					
32	DB8																					
33	DB7																					
34	DB6																					
35	DB5																					
36	DB4																					
37	DB3																					
38	DB2		Fix unused pin to the VSS level																			
39	DB1																					
40	DB0																					
41	VSYNC	Frame-synchronizing signal. (VSPL=0 Low active,VSPL=1 High active) Fix this pin at VSS level if the pin is not used.																				
42	HSYNC	Line-synchronizing signal. (HSPL=0 Low active,HSPL=1 High active) Fix this pin at VSS level if the pin is not used.																				
43	DOTCLK	Input pin for clock signal of external interface:dot clock. DPL=0 Display data is fetched at DOTCLK's rising edge. DPL=1 Display data is fetched at DOTCLK's falling edge. Fix this pin at VSS level if the pin is not used.																				
44	Enable	Data enablesignal pin for RGB interface.																				
		<table border="1"> <thead> <tr> <th>EPL</th> <th>ENABLE</th> <th>GRAM write</th> <th>GRAM address</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Valid</td> <td>Updated</td> </tr> <tr> <td>0</td> <td>1</td> <td>Invalid</td> <td>Held</td> </tr> <tr> <td>1</td> <td>0</td> <td>Invalid</td> <td>Held</td> </tr> <tr> <td>1</td> <td>1</td> <td>Valid</td> <td>Updated</td> </tr> </tbody> </table>	EPL	ENABLE	GRAM write	GRAM address	0	0	Valid	Updated	0	1	Invalid	Held	1	0	Invalid	Held	1	1	Valid	Updated
		EPL	ENABLE	GRAM write	GRAM address																	
		0	0	Valid	Updated																	
		0	1	Invalid	Held																	
1	0	Invalid	Held																			
1	1	Valid	Updated																			

Pin No.	Symbol	Function		
45	SDI	For a serial peripheral interface(SPI),input data is fetched at the rising edge of the SCL signal,Fix SDI pin at VSS level if the pin is not used.		
46	SDO	For a serial peripheral interface(SPI),serves as the serial data output pin(SDO),Successive bits are output at the falling edge of the SCL signal.		
47	CSB	Chip select signal input pin. 0=driver IC is selected and can be accessed. 1=driver IC is not selected and cannot be accessed.		
48	RW_WRB			
		Pin function	CPU type	Pin description
		RW	68-system	Read/Write operation selection pin 0=write 1=read
		WRB	80-system	Write strobe signal.(Input pin)Data is fetched at the rising edge.
		SCL	SPI	The synchronous clock signal
49	RS	Register select pin. 0=Index/status. 1=instruction parameter,GRAM data Must be fixed at VDD3 level when not used.		
50	E_RDB	Pin Function CPU type Pin description		
		E	68-system	Read/Writeoperation enable pin
		RDB	80-system	Read strobe signal. Read out data at the low level
		When SPI mode is selected,fix this pin at VDD3 levle		
51	RESETB	Reset pin initializes the IC when low.Should be reset after power-on.		
52	MVDD	Internal power for RAM.Connect a capacitance to gnd.		
53	VREG1OUT	A reference level for the grayscale voltage.		
54	VCI	Power supply for analog circuit(2.5v~3.3v).		
55	VGH	The positive voltage used in the gate driver.		

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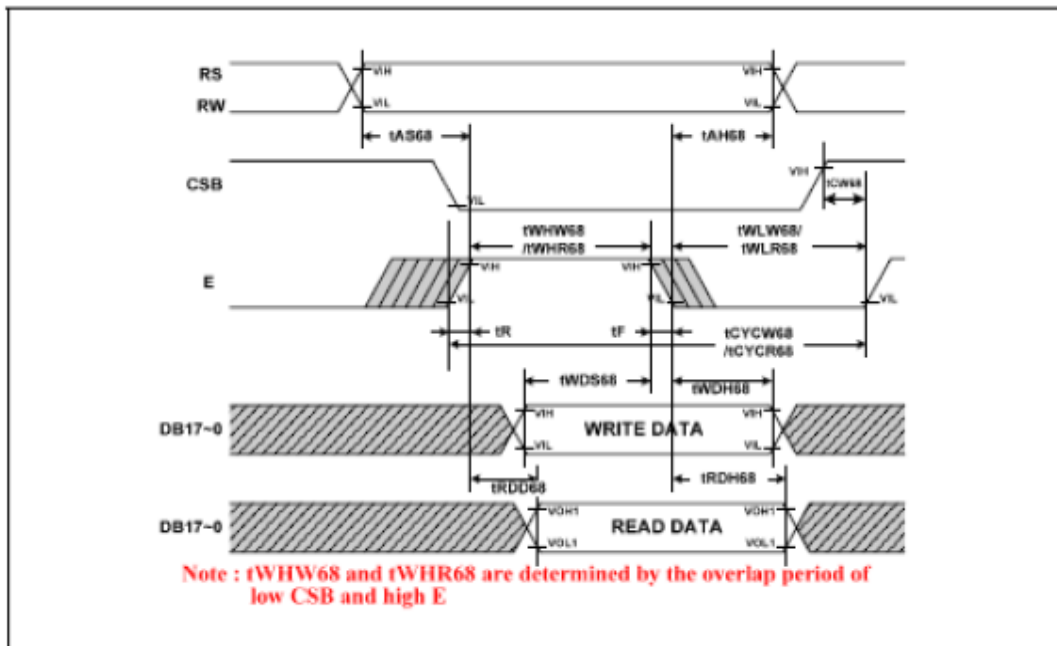
Pin No.	Symbol	Function
56	VGL	The negative voltage used in the gate driver.
57	GND	Ground.
58	TP1	For touch screen.
59	TP2	For touch screen.
60	TP3	For touch screen.
61	TP4	For touch screen.

## 2.3 Timing Characteristics

### CPU Interface M68

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, T<sub>A</sub> = -40 to +85°C)

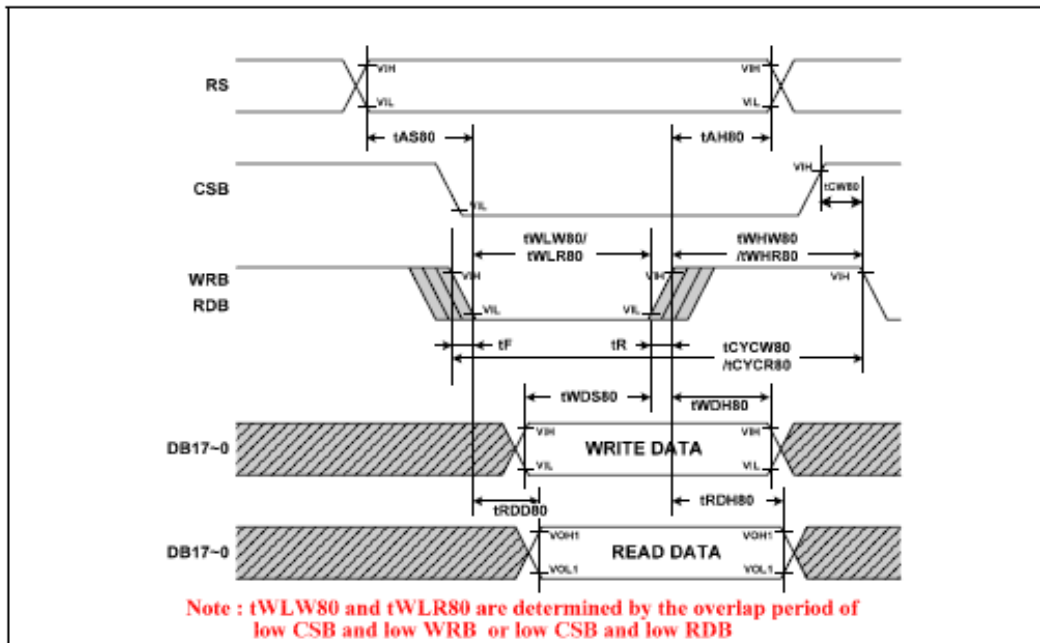
Characteristic	Symbol	Specification		Unit
		Min.	Max.	
Cycle time	Write	t <sub>CYW68</sub>	85	-
	Read	t <sub>CYR68</sub>	500	-
Pulse rise / fall time	t <sub>r</sub> , t <sub>f</sub>	-	15	
Pulse width low	Write	t <sub>WHL68</sub>	27.5	-
	Read	t <sub>WHR68</sub>	250	-
Pulse width high	Write	t <sub>WLH68</sub>	27.5	-
	Read	t <sub>WLR68</sub>	250	-
RS,RW to CSB, E setup time	t <sub>AS68</sub>	10	-	ns
RS,RW to CSB, E hold time	t <sub>AH68</sub>	2	-	
CSB to E time	t <sub>CW68</sub>	15	-	
Write data setup time	t <sub>WDS68</sub>	40	-	
Write data hold time	t <sub>WDH68</sub>	15	-	
Read data delay time	t <sub>RDS68</sub>	-	200	
Read data hold time	t <sub>RDH68</sub>	5	-	



## CPU Interface M80

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, T<sub>A</sub> = -40 to +85°C)

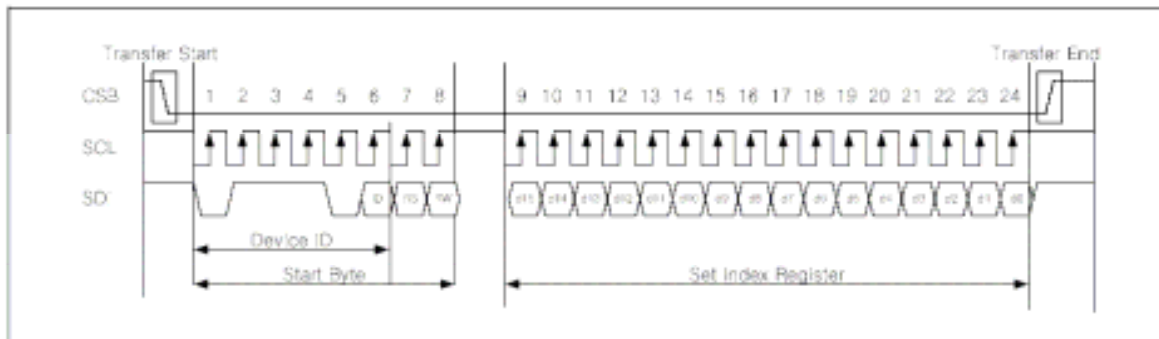
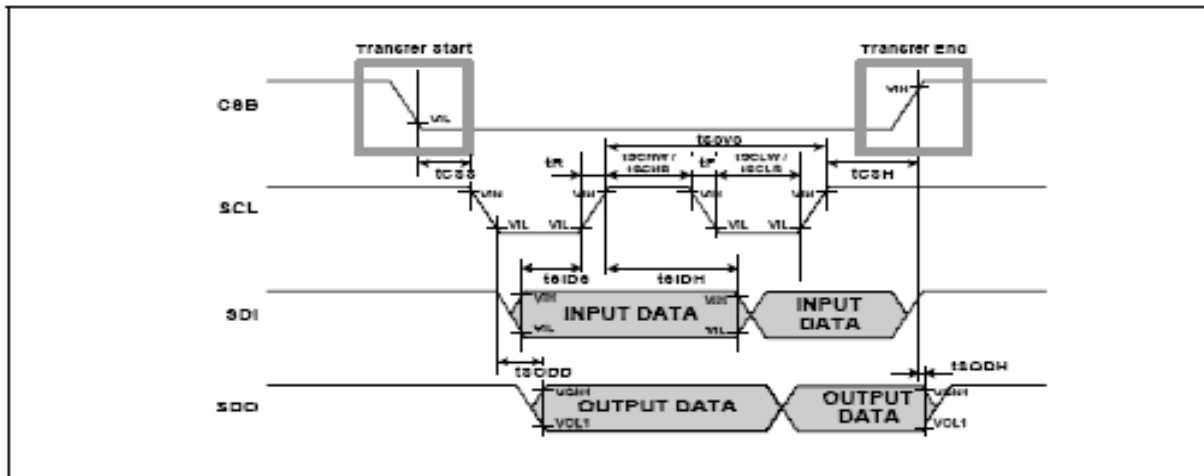
Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	t <sub>CYCWS0</sub>	85	-	ns
	Read	t <sub>CYCRS0</sub>	500	-	
Pulse rise / fall time		t <sub>R</sub> , t <sub>F</sub>	-	15	
Pulse width low	Write	t <sub>WLW80</sub>	27.5	-	
	Read	t <sub>WLR80</sub>	250	-	
Pulse width high	Write	t <sub>WHW80</sub>	27.5	-	
	Read	t <sub>WHR80</sub>	250	-	
RS to CSB, WRB(RDB) setup time		t <sub>AS80</sub>	10	-	
RS to CSB, WRB(RDB) hold time		t <sub>AH80</sub>	2	-	
CSB to WRB(RDB) time		t <sub>OW80</sub>	15	-	
Write data setup time		t <sub>WDS80</sub>	40	-	
Write data hold time		t <sub>WDH80</sub>	15	-	
Read data delay time		t <sub>RDS80</sub>	-	200	
Read data hold time		t <sub>RDH80</sub>	5	-	



## SPI

**Table65: Clock Synchronized Serial Write Mode Characteristics**  
(VDD = 1.5V, VDD3 = 1.65 to 3.3V, T<sub>A</sub> = -40 to +85°C)

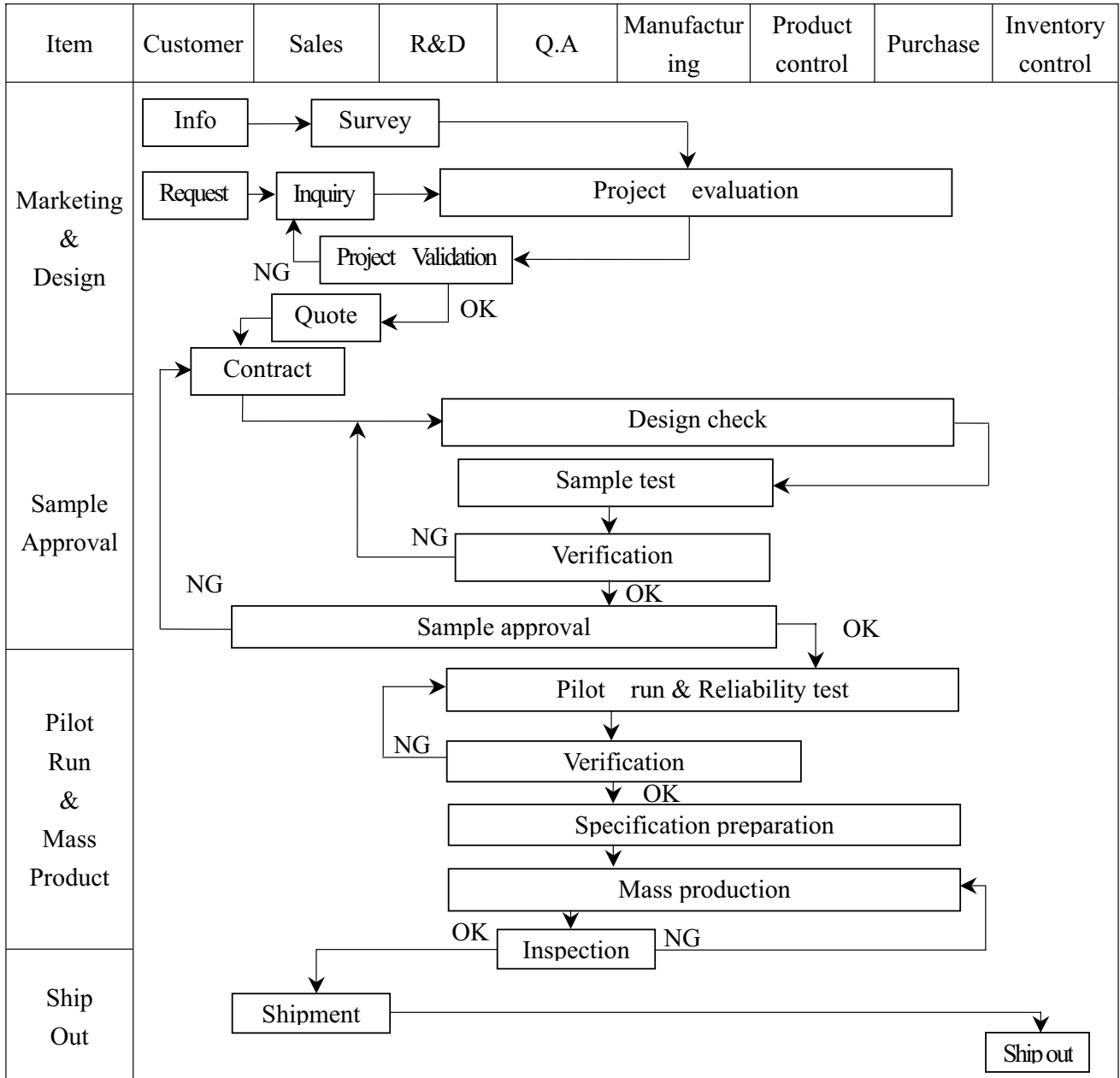
Characteristic	Symbol	specification		Unit
		Min.	Max.	
Serial clock write cycle time	t <sub>scyc</sub>	130	-	ns
Serial clock read cycle time	t <sub>scyc</sub>	250	-	ns
Serial clock rise / fall time	t <sub>r</sub> , t <sub>f</sub>	-	16	ns
Pulse width high for write	t <sub>scHW</sub>	50	-	ns
Pulse width high for read	t <sub>scHR</sub>	110	-	ns
Pulse width low for write	t <sub>scLW</sub>	50	-	ns
Pulse width low for read	t <sub>scLR</sub>	110	-	ns
Chip Select setup time	t <sub>csS</sub>	20	-	ns
Chip Select hold time	t <sub>csH</sub>	60	-	ns
Serial input data setup time	t <sub>siDS</sub>	30	-	ns
Serial input data hold time	t <sub>siDH</sub>	30	-	ns
Serial output data delay time	t <sub>soDD</sub>	-	130	ns
Serial output data hold time	t <sub>soDH</sub>	5	-	ns

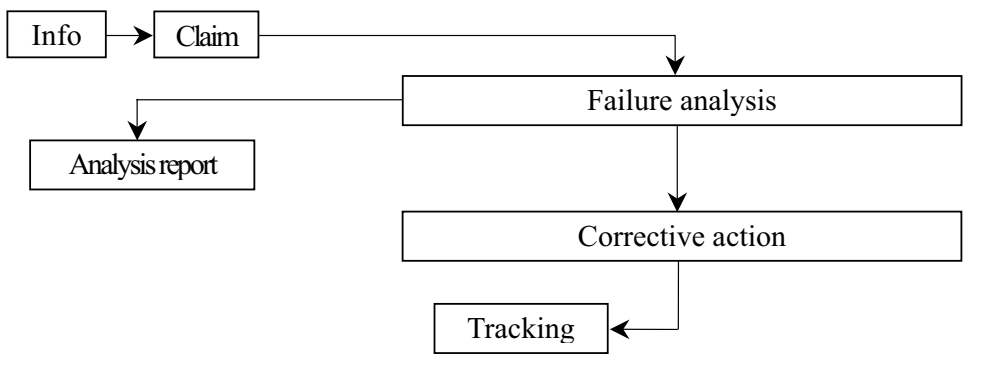




### 3. QUALITY ASSURANCE SYSTEM

#### 3.1 Quality Assurance Flow Chart



Item	Customer	Sales	R&D	Q.A	Manufacturing	Product control	Purchase	Inventory control
Sales Service	 <pre> graph TD     Info[Info] --&gt; Claim[Claim]     Claim --&gt; Failure[Failure analysis]     Failure --&gt; Analysis[Analysis report]     Failure --&gt; Corrective[Corrective action]     Corrective --&gt; Tracking[Tracking]           </pre>							
Q.A Activity	1. ISO 9001 Maintenance Activities 3. Equipment calibration 5. Standardization Management				2. Process improvement proposal 4. Education And Training Activities			

## 4. RELIABILITY TEST

### 4.1 Reliability Test Condition

No.	Items	Specification
1	High Temp.Storage	85°C,240hrs
2	Low Temp.Storage	-40°C,240hrs
3	High Temp.Operation	70°C,240hrs
4	Low Temp.Operation	-20°C,240hrs
5	High Temp/Humidity Storage	85°C,85%RH,240hrs
6	High Temp/Humidity Operation	65°C,90%RH,240hrs
7	Thermal shock	-40°C~85°C (-40°C /30min;transit /3min;85°C /30min;transit /3min)1 cycle:66min,100 cycles
8	Peel strength	>500g/cm(Speed~50mm/min)
9	Vibration	Frequency:5~50HZ,0.5G
		Scan rate:1 oct/min
		Time:2hrs/axis
		Test axis:X,Y,Z
10	Drop	Hight:120cm
		Sequence:1angle、3edges and 6 faces
		Cycles:1
11	ESD	Air discharge model,+/-8kV,10 times

#### Evaluation Criteria

- \_ No damage to glass or encapsulation
- \_ No drastic change to display
- \_ Pixel/Line defects:no increased
- \_ Luminance:Within+/-50% of initial value
- \_ Uniformity:(Max-Min)/Min<15%
- \_ Current consumption:within +/-50%of initial value

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## 5. PRECAUTION RELATING PRODUCT HANDLING

### 5.1 SAFETY

- 5.1.1 If the LCD panel breaks , be careful not to get the liquid crystal to touch your skin.
- 5.1.2 If the liquid crystal touches your skin or clothes , please wash it off immediately by using soap and water.

### 5.2 HANDLING

- 5.2.1 Avoid any strong mechanical shock which can break the glass.
- 5.2.2 Avoid static electricity which can damage the CMOS LSI—When working with the module , be sure to ground your body and any electrical equipment you may be using.
- 5.2.3 Do not remove the panel or frame from the module.
- 5.2.4 The polarizing plate of the display is very fragile. So , please handle it very carefully, do not touch , push or rub the exposed polarizing with anything harder than an HB pencil lead (glass , tweezers , etc.)
- 5.2.5 Do not wipe the polarizing plate with a dry cloth , as it may easily scratch the surface of plate.
- 5.2.6 Do not touch the display area with bare hands , this will stain the display area.
- 5.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.
- 5.2.8 To control temperature and time of soldering is  $320 \pm 10^{\circ}\text{C}$  and 3-5 sec.
- 5.2.9 To avoid liquid (include organic solvent) stained on LCM

### 5.3 STORAGE

- 5.3.1 Store the panel or module in a dark place where the temperature is  $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$  and the humidity is below 65% RH.
- 5.3.2 Do not place the module near organics solvents or corrosive gases.
- 5.3.3 Do not crush , shake , or jolt the module.

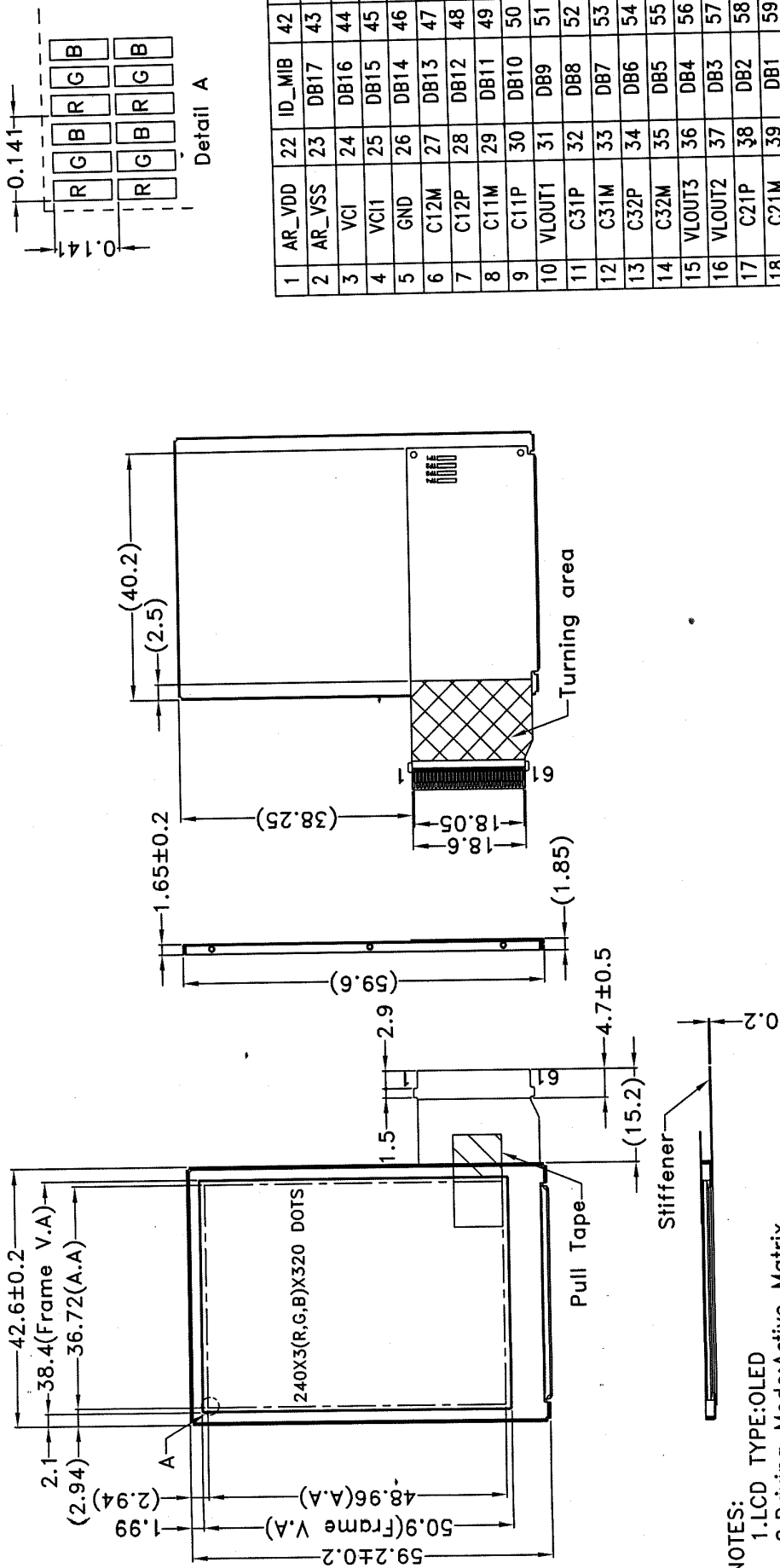
### 5.4 TERMS OF WARRANTY

#### Unaccepted responsibility

This product has been manufactured to your company's specification as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in nuclear power control equipment, aerospace equipment , fire and security systems or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required.

## 6. PACKING Specification

\* See Appendix



- NOTES:
- 1.LCD TYPE:OLED
  - 2.Driving Mode:Active Matrix
  - 3.Color Mode:Full Color(262K color)
  - 4.Top: -20~70°C Tst:-40~85°C
  - 5.The tolerance unless classified ±0.3mm
  - 6.Diagonal Size:2.4"(Inch)
  - 7.Driver IC:S6E63D6,COG Assembly
  - 8.Connector : HIROSE FH23-61S-0.3SHW(05)

1	AR_VDD	22	ID_MIB	42	HSYNC
2	AR_VSS	23	DB17	43	DOTCLK
3	VCI	24	DB16	44	ENABLE
4	VCI1	25	DB15	45	SDI
5	GND	26	DB14	46	SDO
6	C12M	27	DB13	47	CSB
7	C12P	28	DB12	48	RW_WRB
8	C11M	29	DB11	49	RS
9	C11P	30	DB10	50	E_RDB
10	VLOUT1	31	DB9	51	RESETB
11	C31P	32	DB8	52	MVDD
12	C31M	33	DB7	53	VREGTOUT
13	C32P	34	DB6	54	VCI
14	C32M	35	DB5	55	VGH
15	VLOUT3	36	DB4	56	VGL
16	VLOUT2	37	DB3	57	GND
17	C21P	38	DB2	58	TP1
18	C21M	39	DB1	59	TP2
19	VGS	40	DB0	60	TP3
20	IOVCC	41	VSYNC	61	TP4
21	SPB				

圖面名稱	RH240320L-2X4NN-O	SCALE:1/1	UNIT:mm	PAGE:1/1	APPROVED	CHECKER	DRAWN
圖面編號	PPT-06002-007						
ED	A						
REV							
DATE	JUN/11/07						
DESCRIPTION	Modify FPC outline						

2-060-01-01

LCM Model

RH240320L-2X4NN-O

版次Ver.A

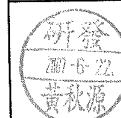
# LCM包裝規格書

## LCM Packaging Specifications

Approve

Check

Contact



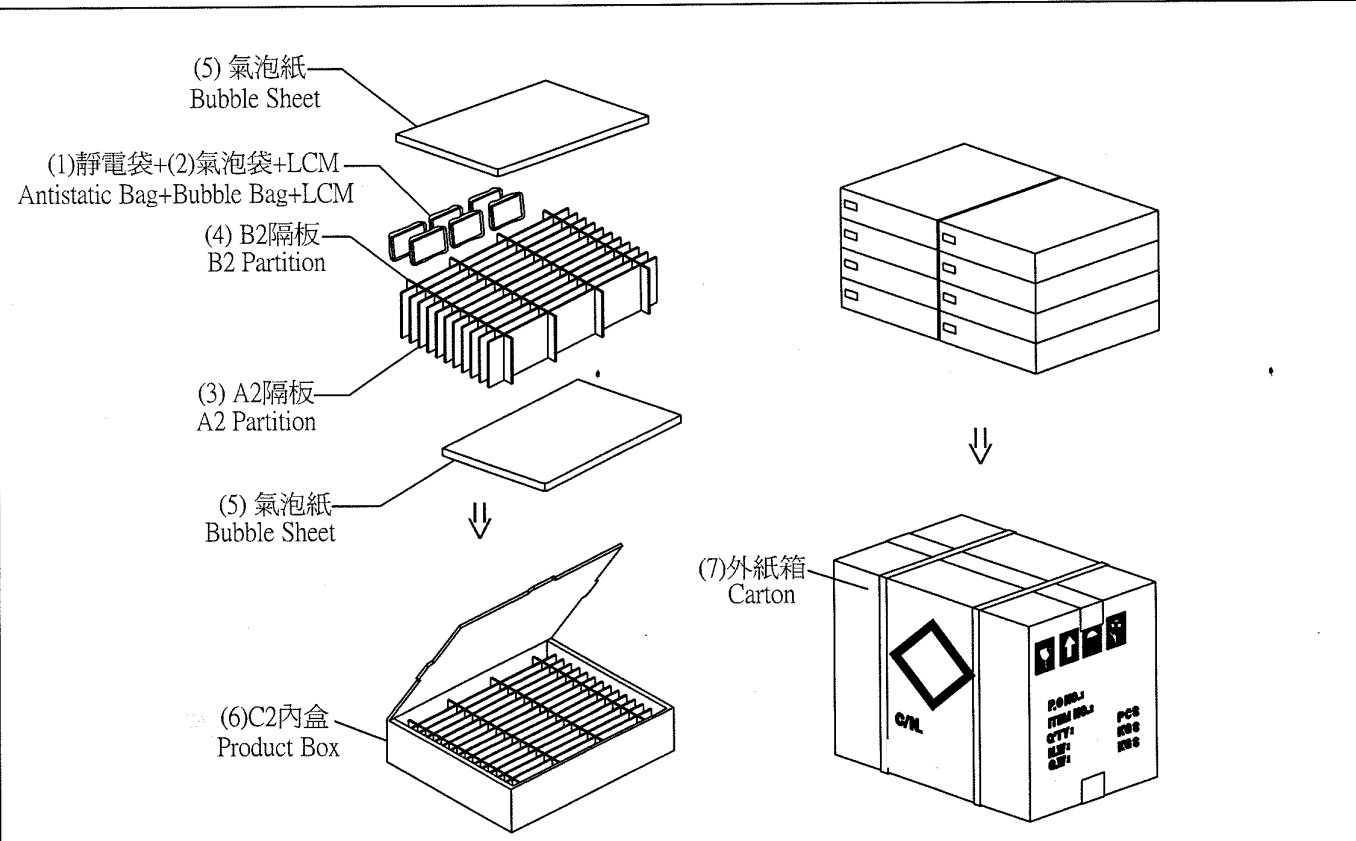
### 1. 包裝材料規格表 (Packaging Material) : (per carton)

No.	Item	Model	Dimensions (mm)	Quantity
1	成品 (LCM)	RH240320L-2X4NN-O	50.0 X 68.0	288
2	靜電袋(1)Antistatic Bag	BAG100100ARABA	100 X 100	288
3	氣泡袋(2)Bubble Bag	BAG100080BWABA	1000 X 80	288
4	A2隔板(3)A2 Partition	BX29300070BMBA	293 X 70 X 2.5	88
5	B2隔板(4)B2 Partition	BX24500070BLBA	245 X 70 X 2.5	32
6	氣泡紙(5)Bubble Sheet	BAG280240BWABA	280 X 240	16
7	C2內盒(6)Product Box	BX31025580AABA	310 X 255 X 80	8
8	外紙箱(7)Carton	BX52732536CCBA	527 X 325 X 360	1
9				

### 2. 單箱數量規格表 (Packaging Specifications and Quantity) :

(1)Quantity Of Spacer : A2隔板 X 11 , B2隔板 X 4

(2)Total LCM quantity in carton : quantity per box 36 x no of boxes 8 = 288



### 特 記 事 項 (REMARK)

#### 1. Label Specifications :

MODEL:  
LOT NO:  
QUANTITY:  
CHECK:

